

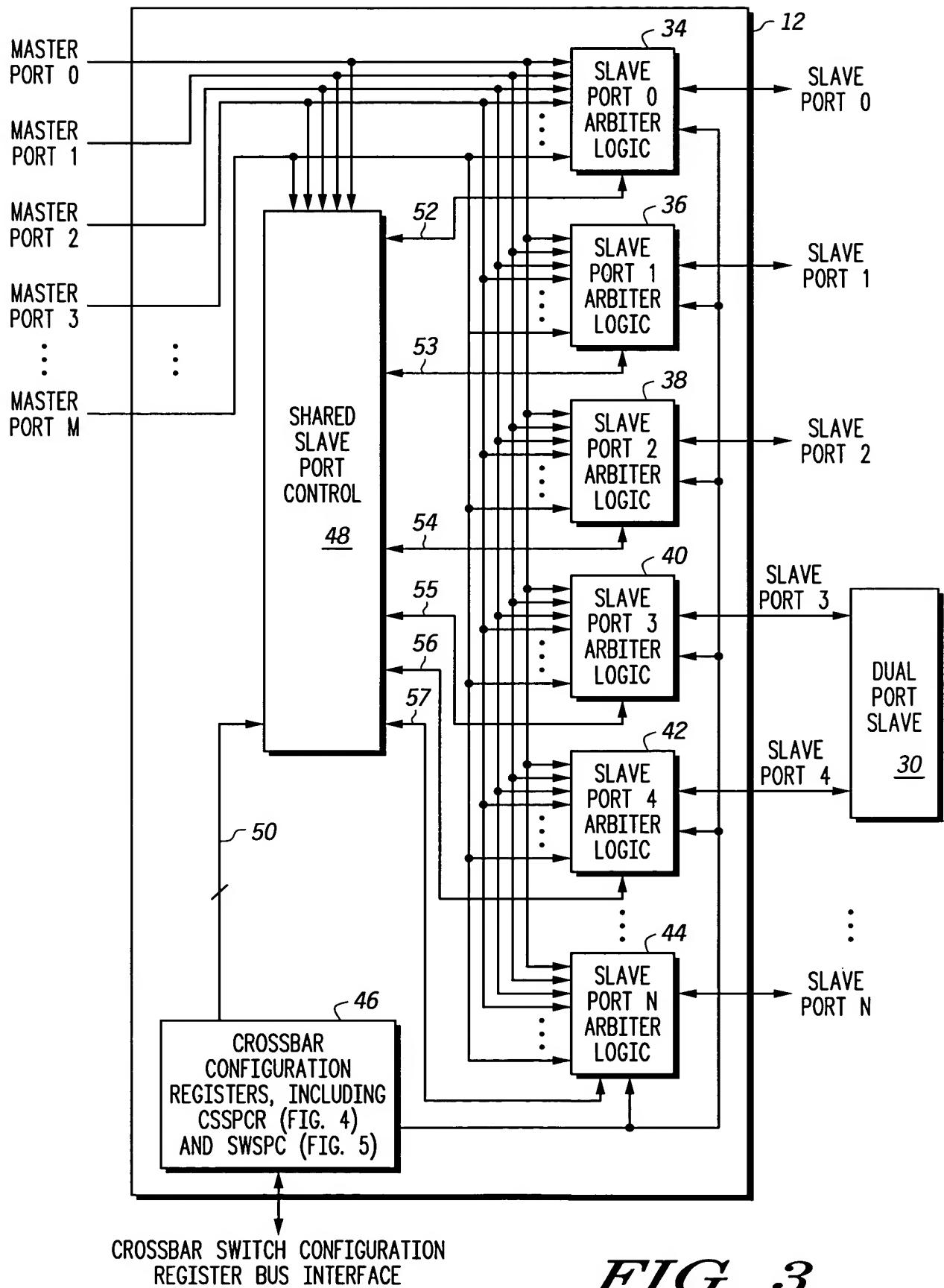
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FIG. 1

MEMORY MAP

SLAVE PORT 0 : 0x0000_0000 - 0x1FFF_FFFF
SLAVE PORT 1 : 0x2000_0000 - 0x4FFF_FFFF
SLAVE PORT 2 : 0x5000_0000 - 0x5FFF_FFFF
SLAVE PORT 3 : 0x6000_0000 - 0x6FFF_FFFF (SHARED)
SLAVE PORT 4 : 0x6000_0000 - 0x6FFF_FFFF (SHARED)

FIG. 2



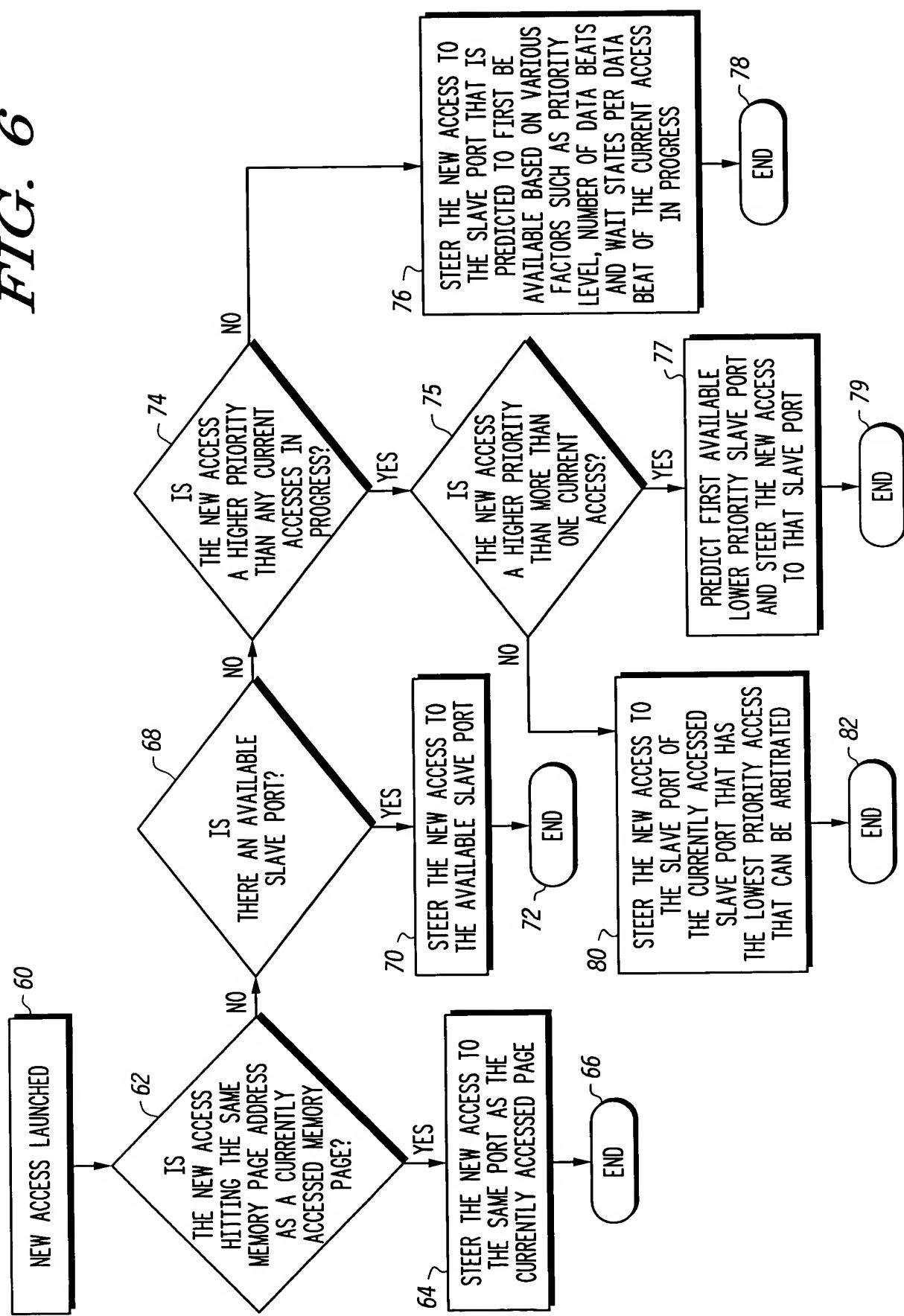
CROSSBAR SHARED SLAVE PORTS CONTROL REGISTER																
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NAME	MP7	MP6	MP5	MP4	MP3	MP2	MP1	MP0								
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	SIZE				PAGES				SSP							

FIG. 4

SLAVE PORT WAIT-STATE PREDICTION CONTROL																
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NAME	SLV9WS	SLV8WS	SLV7WS	SLV6WS	SLV5WS	SLV4WS	SLV3WS	SLV2WS	SLV1WS	SLV0WS						
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME																

FIG. 5

FIG. 6



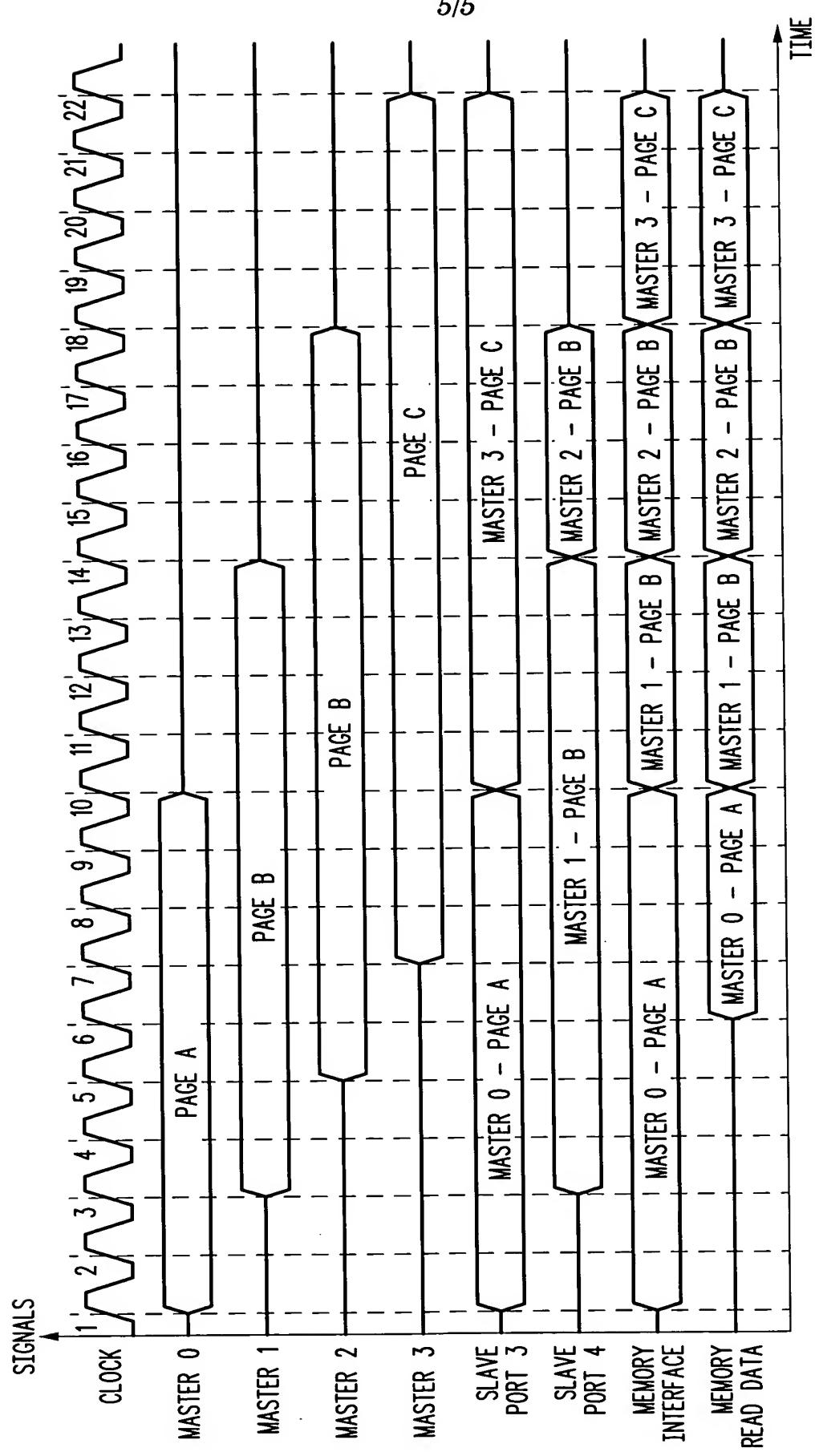


FIG. 7